a single switcher that connects each of the plural processing elements to each other,

wherein each of the plural processing elements includes a network interface and is connected to the single switcher via the network interface.--

Amend claim 2 as follows:

--2. (amended) The semiconductor device of claim 1, wherein the plural processing elements are located around the single switcher.--

Amend claim 4 as follows:

--4. (amended) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single semiconductor chip.--

Amend claim 5 as follows:

--5. (amended) The semiconductor device of claim 1, wherein the plural processing elements and the single switcher are implemented in a single package.--

Amend claim 6 as follows:

--6. (amended) The semiconductor device of claim 1, wherein one of the plural processing elements and the single switcher are connected by peer-to-peer connection via at least one transmission line.--

Amend claim 7 as follows:

--7. (amended) The semiconductor device of claim 1, wherein each of the plural processing elements has a function of the same hierarchical level.--

Amend claim 8 as follows:

--8. (amended) The semiconductor device of claim 1, wherein at least one of the plural processing elements and the single switcher are located in a space where light is confined, and each of the at least one of the plural processing elements and the single switcher has a light emitting element and a light receiving element, wherein an optical communication is performed between the at least one of the plural processing elements and the single switcher.--

Amend claim 9 as follows:

--9. (amended) The semiconductor device of claim 1 further comprising:

a plurality of semiconductor chips each of which includes plural processing elements and a single switcher; and

at least one inter-switcher which connects the semiconductor chips to each other.--

Amend claim 10 as follows:

--10. (amended) The semiconductor device of claim 9, wherein the plural semiconductor chips and the inter-switcher are implemented on a single package.--

Amend claim 11 as follows:

--11. (amended) The semiconductor device of claim 9, wherein the inter-switcher is located in one of the plural semiconductor chips, and the plural semiconductor chips are implemented on a plurality of stacked packages.--

Add the following new claims:

--13. (new) The semiconductor device of claim 1, wherein each of the plural processing elements are only connected to the single switcher, through each respective network interface.

--14. (new) A semiconductor device comprising:

a plurality of peripheral input/output processing elements;

a core processor; and

a single switcher that connects each of the plural peripheral processing elements and the core processor to each other,

wherein each of the plural peripheral processing elements and the core processor includes a network interface and are connected to the single switcher via a respective network interface.--

REMARKS

A proposed drawing correction is submitted for Figure 4 to address a drawing objection noted in the Official Action.